TITLE OF INVENTION

Integrated anneal cap/ ion implant mask/ trench isolation structure for III-V devices.

INVENTORS

David A. Johnson, Charles W. Jurgensen

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] N/A

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0002] This Invention was not conceived, constructed, or tested during the performance of a government contract.

REFERENCE TO SEQUENCE LISTING, A TABLE, OR A COMPUTER PROGRAM LISTING COMPACT DISK APPENDIX

[0003] N/A

BACKGROUND OF THE INVENTION

Field of invention

[0004] The present invention relates broadly to III-V semiconductor devices, and in particular, an improved isolation structure for such devices

Description of the prior art

[0005] The composite dielectric layer used in the fabrication of III-V devices, disclosed in U.S. patent 5,001,076, has been instrumental in yielding high levels of integration on such semiconductors. As transistor densities increase, and dimensions decrease, there becomes an increasing trade-off between the ability of the dielectric layer to mask ion implantations, and topography resulting from patterning of the composite layer.

[0006] Traditionally mesa-type isolation structures of III-V bipolar transistors are defined after the patterning of the emit-

ter and other device layers as described on p. 375 of S.M. Sze, "High-Speed Semiconductor Devices", Wiley, New York, 1990. The resulting isolation topography greatly complicates the interconnect of these devices. High levels of device integration have not been achieved for III-V bipolar transistors with these isolation last process integration schemes.

[0007] Structures, often referred to as "shallow trench isolation" used in silicon processing to reduce topography rely on silicon specific etches, thermal oxidation to round the trench corners, and do not provide the necessary capping layer required by III-V semiconductors. Examples of these isolation structures are given is U.S. patents 6,500,726; 6,479,369; 6,452,246; 6,177,333; 6,069,057; 6,054,343; 4,980,306; 4,836,885; 4,837,178; 6,265,743. Such structures are also not compatible with III-V semiconductors, and they require the use of a wet etch to remove the final dielectric covering the active regions. Wet etches have disadvantages such as high interfacial etch rates resulting in increased defect densities.

[0008] Isolation structures using oxygen implants, or oxygen doped epitaxial layers such as those disclosed in U.S. patents 5,482,872 and 5,844,303, exhibit higher leakage currents and higher parasitic capacitance.

[0009] Groove isolation structures as disclosed in U.S. patent 5,293,061 do not provide the planarity necessary for defining subsequent fine geometries.

[0010] Structures created for silicon substrates with some components similar to those compatible with III-V compounds such as that disclosed in U.S. patent 6,441,444 require a thermal oxidation step, and subsequent thermal nitridation steps that are incompatible with III-V compounds.

BRIEF SUMMARY OF THE INVENTION

[0011] A trench structure used to isolate III-V devices, as well as act as an anneal cap and ion implant mask is produced with the following procedure:

1. Defining active regions of semiconductor (10) by etching areas (12) around the active regions (11) with a III-V semiconductor etch process leaving the cross-section shown in FIG 1.
2. Depositing a dielectric layer on the wafer suitable for both an anneal cap and CMP stop (13), then depositing a gap fill layer (14) as shown in FIG 2. For devices requiring ion implantation, the combination of the gap fill layer, and the anneal cap/CMP stop layer may also be used as an ion implant stop
3. Polishing the Gap fill layer, and some of the CMP stop layer, leaving the cross-section shown in FIG 3.
4. Removing the CMP stop layer (13) from the top of the III-V semiconductor with an etch selective to the III-V semiconductor, leaving a cross-section shown in FIG 4.

[0012] The resulting structure is significantly more planar than the traditional composite dielectric structure used with III-V VLSI devices. This structure allows for reduced device-level metal capacitance, low active area to active area leakage, and topography reduction compared to conventional III-V bipolar structures. Finally, this structure is compatible with III-V semiconductors, and allows for use of a dry etch for removal of the final dielectric layer over the active semiconductor, where traditional silicon structures do not.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

[0013] FIG 1 is a schematic sectional view of the partially fabricated isolation structure after the isolation etch step.

[0014] FIG 2 is a schematic sectional view of the partially fabricated isolation structure after the deposition of the combination anneal cap layer, and the gap fill layer.

[0015] FIG 3 is a schematic sectional view of the partially fabricated isolation structure after the polishing of the gap fill layer, and part of the combination anneal cap layer.

[0016] FIG 4 is a schematic sectional view of the complete isolation structure.

DETAILED DESCRIPTION OF THE INVENTION

[0017] While the description below is specifically directed to gallium arsenide (GaAs) devices, it will be appreciated that other III-V devices will similarly benefit from the teachings of the invention.

First Embodiment

[0018] The GaAs wafer (10) shown in FIG 1 is either semi-insulating (near intrinsic), or is doped of the opposite type to be used in the outer portions of the active regions (11).

[0019] The wafer is patterned with conventional photolithographic means, and an etch that leaves 500A-5000A deep isolation trenches in the GaAs. The FIG 1 drawing shows sharp bottom corners, but the GaAs etch used at this step will need to round these corners to a degree dictated by the modulus of the gap fill material, and the temperature of subsequent anneals used.

[0020] An optional background implant may be done at this point.

[0021] Next silicon nitride (13) is deposited on the semiconductor as a combination anneal cap layer, and a CMP stop layer. The thickness of this layer is typically 5-25% of the depth of the trench etched, but specifically depends on the uniformities and selectivities of the subsequent process steps.

[0022] A silicon dioxide gap fill layer (14) is deposited on top of the anneal cap layer at a thickness greater than the depth of the isolation trenches.

[0023] An optional anneal may be done at this point to activate the optional background implant, and/ or prepare the gap fill material for further processing.

[0024] An optional photolithographic step is done at this point essentially matching the pattern of that used to define the isolation trenches, but with the image reversed. If this optional photolithographic step is performed, then it is followed by an etch that removes the gap fill dielectric (14) over most of the active region area (11).

[0025] The remaining gap fill dielectric (14) above the active area anneal cap layer (13) is removed with a conventional chemical mechanical polish process resulting in the FIG 3 cross-section.

[0026] The anneal cap is removed from the active regions with an etch selective to GaAs such as a low energy NF3 plasma. This will leave a surface that is planar to the degree of the thickness of the anneal cap layer. The final active area (11)/ isolation region (12) step height will depend on the etch selectivity of the anneal cap removal etch to the gap fill material, and the effect of subsequent etching on the device. The aggregate of these processes may be matched for near perfect planarity as shown in FIG 4.

[0027] The remaining portion of the circuit may then be fabricated on top of the planar surface without concern of device leakage caused by uncapped semiconductor in the isolation regions, and without concern of device leakage caused by implanting active species between the active regions.

Second Embodiment

[0028] The GaAs wafer shown in FIG 1 comprising a substrate, and device epitaxial layers grown on top. Device epitaxial layers may be those used for forming HBT devices, HEMT devices, optimized MESFET devices, or other devices.

[0029] To electrically isolate active regions of the wafers, the wafer is patterned with conventional photolithographic means, and an etch that removes the active layers of the wafer in the isolation regions (12). Depending on the epitaxial structure of the starting material, the depth of these trenches may be anywhere from 500A to several microns.

[0030] Next, silicon nitride (13) is deposited on the semiconductor as a combination anneal cap layer, and a CMP stop layer. The thickness of this layer is typically 5-25% of the depth of the trench etched, but specifically depends on the uniformities and selectivities of the subsequent process steps.

[0031] A silicon dioxide gap fill layer (14) is deposited on top of the anneal cap layer at a thickness larger than the depth of the isolation trenches.

[0032] An optional anneal may be done at this point to prepare the gap fill material for further processing.

[0033] An optional photolithographic step is done at this point essentially matching the pattern of that used to define the isolation trenches (12), but with the image reversed. If this optional photolithographic step is performed, then it is followed by an etch that removes the gap fill dielectric (14) over most of the active region area.

[0034] The remaining gap fill dielectric above the active area anneal cap layer is removed with a conventional chemical mechanical polish process.

[0035] The anneal cap (13) is removed from the active regions with an etch selective to the top epitaxial layer such as a low energy NF3 plasma. This will leave a surface that is planar to the degree of the thickness of the anneal cap layer.The final active area/ isolation region step height will depend on the selectivity of the anneal cap removal etch to the gap fill material, and the effect of subsequent etching on the device. The aggregate of these processes may be matched for near perfect planarity as shown in FIG 4.

[0036] The remaining portion of the circuit may then be fabricated on top of the planar surface without concern of device leakage caused by uncapped semiconductor in the isolation regions, remaining active layers between active regions, or implanting active species between the active regions.